REMARKS

In the Office Action, the Examiner indicated that claims 1 through 8 are pending in the application. The Examiner objected to claims 4, 5, 7, and 8 and rejected claims 1-3 and 6.

Applicant acknowledges the Examiner's comments regarding unclaimed features and has amended claim 1 to more specifically recite the exclusive storing of data in the parameter RAM of data for populating variables of programming instructions for use in programming instructions stored elsewhere.

The Present Invention

The present invention relates to a hardware accelerator, e.g., as used in a DSP that is provided with a parameter RAM memory exclusively for storing data for populating variables of programming instructions for use in programming instructions stored elsewhere. An example of such variables are the parameters required for the various operating conditions of the accelerator. In a DSP application, the DSP can easily and without hardware modification accommodate design changes such as the need to support additional ADSL lines.

More particularly, in a preferred embodiment, the invention is a digital signal processor (DSP), comprising a hardware accelerator and a parameter RAM coupled to the hardware accelerator, the parameter RAM storing operating condition parameters for use by the hardware accelerator. In another preferred embodiment, the DSP is used in connection with a communication system employing plural ADSL

lines, and the parameter RAM is configurable to store operating condition parameters for each of the plurality of ADSL lines.

U.S. Patent No. 4,839,851 to Maki

U.S. Patent No. 4,839,851 to Maki ("Maki") teaches a programmable data path device capable of operating as a general purpose hardware accelerator. The device of Maki includes a program memory 14 and a data path module 12. Program memory 14 comprises a standard digital random access memory (RAM). The program memory 14 is coupled to data path module 12. Program memory 14 stores a plurality of programming instructions (process control words) that are sequentially provided to data path module 12 via bus 26. The programming instructions define the control states of device 10, and control the operation of data path module 12.

Claim Rejections, 35 U.S.C. §102

On page 2 of the Office Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. §102(a), (b) as being anticipated by U.S. Patent No. 4,839,851 to Maki ("Maki").

The Cited Prior Art Does Not Anticipate the Claimed Invention

The MPEP and case law provide the following definition of anticipation for the purposes of 35 U.S.C. §102:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 citing *Verdegaal Bros. v. Union Oil Company of California*, 814 F.2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)

The Examiner Has Not Established a *prima facie* Case of Anticipation

As noted above, the present claimed invention includes a parameter RAM coupled to a hardware accelerator. A parameter RAM is a specific type of RAM that simply saves data (parameters) pertaining to variables, not programming instructions. The parameters stored in the parameter RAM are used to populate variables in programming instructions that are stored somewhere other than in the parameter RAM. This allows the program instructions and control words to be hard-coded, thereby requiring less memory and thus consuming less space. The combination of hardware accelerator and parameter RAM can form a digital signal processor appropriate for many uses, particularly for use in a communication system employing plural ADSL lines.

The program memory 14 in Figure 2 of Maki is not equivalent to the parameter RAM of the present invention. The program memory 14 of Figure 2, as described in Maki, merely performs normal program memory functions, that is, it stores program instructions/control words for execution.

By contrast, the parameter RAM of the present invention does not store standard programming instructions; rather, the parameter RAM of the present invention exclusively stores data to be used in variables of the programming instructions (stored elsewhere), for example, hard-coded into the system. By varying the parameters instead of the program instructions (as is done in Maki), the present invention is optimized for size. Nothing in Maki teaches or suggests the use of a parameter RAM, as is claimed in the present invention, and none of the elements described by the Examiner performs the function of the parameter RAM of the present invention. Thus, for this reason alone, independent claim 1, and all claims depending therefrom, patentably define over Maki.

In addition, the present invention requires the coupling of the parameter RAM described above to a hardware accelerator. Contrary to the Examiner's assertion, the data path module 12 of Figure 2 is not a hardware accelerator. Data path module 12 simply receives data via input bus 20, and processes the data to produce output data on output bus 22. Nothing in Maki teaches or suggests use of a hardware accelerator for data path module 12. Without such a teaching, Maki does not anticipate the claimed invention. For this reason, in addition to those above, claim 1 and all claims depending therefrom is allowable over Maki.

Applicant acknowledges that the entire configuration of Maki finds use as a hardware accelerator. However, this fact does not anticipate the present invention, whereby a hardware accelerator is coupled with a parameter RAM to optimize the area consumed by, for example, a digital signal processor.

Rejection of Claims 3 and 6 under 35 U.S.C. §103(a)

On page 2 of the Office Action, the Examiner rejected claims 3 and 6 under 35 U.S.C. §103(a) as being unpatentable over Maki in view of U.S. Patent No. 5,883,907 to Hoekstra.

As noted above, claim 1, and all claims depending therefrom (including claims 3 and 6) are patentably distinct from Maki. The addition of Hoekstra does not render claims 3 and 6 obvious. Nothing in Hoekstra teaches or suggests the combining of a parameter RAM with a hardware accelerator, as is claimed in claims 3 and 6. Accordingly, claims 3 and 6 also patentably define over the prior art, for the reasons set forth above.

Conclusion

The present invention is not taught or suggested by the prior art. Accordingly, the Examiner is respectfully requested to reconsider and withdraw the rejection of the claims. An early Notice of Allowance is earnestly solicited.

Enclosed herewith, in triplicate, is a Petition for extension of time to respond to the Examiner's Action. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment associated with this communication to Deposit Account No. 19-5425.

Respectfully submitted

2/2/04
Date

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